Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **D3**
2. **D2**
3. **D1**
4. **D0**
5. **Y**
6. **W**
7. **N/C**
8. **GND**
9. **C**
10. **B**
11. **A**
12. **D7**
13. **D6**
14. **D5**
15. **D4**
16. **VCC**

**.060”**

**14**

**13**

**12**

**11**

**10**

**2 1 16 15**

**3**

**4**

**5**

**6**

**7 8 9**

**HC151E**

**MASK**

**REF**

**.067”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: VCC**

**Mask Ref: HC151E**

**APPROVED BY: DK DIE SIZE .060” X .067” DATE: 7/11/22**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: 54HC151**

**DG 10.1.2**

#### Rev B, 7/1